FPGA Pixel Array Detector

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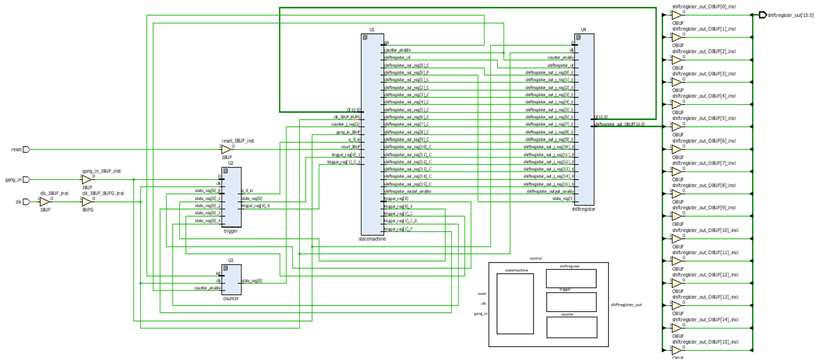
Acronyms

- FPGA : Field Programmable Gate Array
- PAD : Pixel Array Detector
- ASIC : Application Specific Integrated Circuit
- PCB : Printed Circuit Board
- TSI : Through Silicon Interconnect
- ACF : Autocorrelation Function
- CMOS : Complementary Metal-Oxide-Semiconductor
- VHDL : Very high speed integrated circuit Hardware Design Language

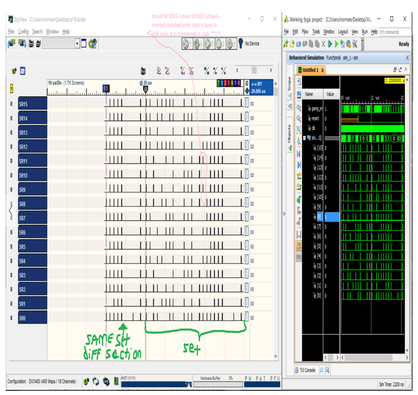
FPGA program in schematic form using VHDL and a basic visual diagram of VHDL design



Description of schematic components

- Control (most outer box) - serves as the unit that ultimately allows what things to come in and what finally goes out. Additionally, it acts as a unit in which signals of other components inside it, can communicate to each other within
- Shiftregister – receives the incoming data bit as it comes in by shifting the last bit it has received to the next slot (16 slots per pixel gang). It will keep shifting the data bits until the counter counts to 16
- Trigger – receives "10", which indicates to the system that an incoming pixel gang is imminent
- Counter – once the "10" comes into the FPGA system from the ASIC chip, the counter will count to 16, indicating the registers are now fully acquitted with data
- Statemachine – controlling the state of the system within. It signals the system what stage it is in: idle – when system first initiates, waiting – when the system is waiting for the trigger, receiving – when the system is registering the incoming data bits, data_valid – when the system can output the stored data in the shiftregister. It also resets the counter and shiftregister after each pixel gang

Results



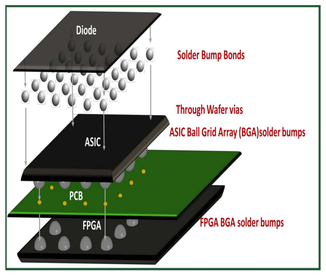
- Simulation(program on right) – with a made up data set, the simulation was successful in terms of replicating the desired data set with the addition of false trigger bits to rule out false data sets prompted by undesired signals
- Real life trial(program on left) – this data, result of using the logic analyzer, had its inputs connected to the FPGA board (Nexys 4) output pins itself. The output of the logic analyzer is connected to the computer in order to run the Digiview software to analyze the signals. The results were exactly the same disregarding some clerical error made; indicating it would work in the real-world

Problem

- Project was born out of the need to process data in real time from X-ray machines
- The biggest problem that X-ray scientists face today is…….

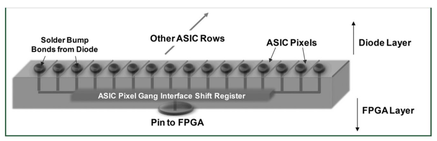
Getting the data home!!

FPGA PAD Process



1. X-ray photons are received through the diode layer and is converted to charge
2. Next, through the solder bonds, the ASIC layer converts this charge into a voltage, assisted by a comparator. It is then outputted as a single bit
3. Bits are then streamed through the massively parallel interface (PCB) for accurate data inputs into the FPGA pins

4. Pixels are arranged into "pixel gangs", so that each pin connection from the ASIC to the FPGA passes sixteen bits

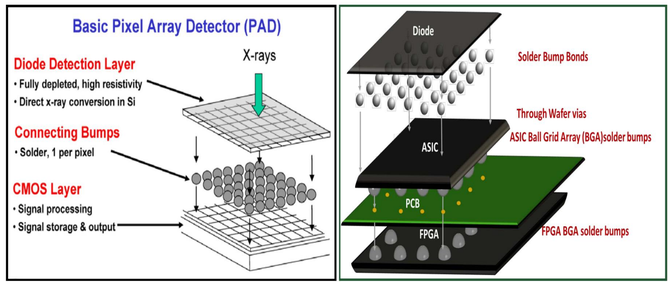


5. Once the data bits go into the FPGA chip in pixel gangs, the data will be processed and sent to a storage device

Conclusion

X-ray scientists today, face the problem of getting real-time data efficiently. This prompts the creation of a FPGA PAD system to process data in real-time to get almost instant results. Real-time results are made possible by the fast parallel computing capabilities of the FPGA chip. Using the data from the results, a software program can be used to convert the signals into a more user friendly interface – like an x-ray photo that people are used to seeing. Though the FPGA programming evidently shows great results in terms of intended functionality, the whole project as a whole can use improvements to: optimize ACF data collection for different classes of experiments, making the FPGA a smaller footprint, implement a cooling solution for the detector, and developing a simple protocol to communicate between different layers of the PAD.

Current PAD Conceptual FPGA PAD



Advantages

Current PAD

- High spatial and temporal resolution
- Good signal-to-noise ratio
- ASIC layer allows for in-pixel signal processing

FPGA PAD

- Cheaper to produce than traditional IC detector
- Reconfigurable so detector doesn't have to change with each application
- Powerful computing power allows for post processing to be done in real-time instead of a external computing machine, reducing data stored in storage

Disadvantages

Current PAD

- Tend to be application specific
- Hardwired pixels may be large and complex
- Restriction of maximum frame rate of the PAD
- Huge data storage needed for processing
- High speed switching data lines susceptible to noise

FPGA PAD

- FPGA footprint much larger than detector
- Susceptible to high temperatures due to the detector being in close proximity with FPGA
- Trade-off between FPGA resources and precision of ACF

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7. More information on whole project scope: http://bigbro.biophys.cornell.edu/publications/284%20Hromalik.pdf

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  - -Digilent Nexys 4 Artix-7 FPGA Board